## $Ga_2O_3$-based devices

**PIs** Klaus Irmscher (C4.4), Günter Wagner (C3.5), Zbigniew Galazka (C3.1),
Joachim Würfl (associate partner FBH)

**Research team** Michele Baldini, Andreas Fiedler

**Cooperation Partners:** Leibniz-Institut für Kristallzüchtung; Air Force Research Lab, Ohio;
Ferdinand-Braun Institut

GraFOx is primarily dedicated to improving materials perfection with the goal to demonstrate and understand their fundamental properties. Yet, the optimized materials achieved within GraFOx are used to realize devices together with associated partners (Ferdinand-Braun-Institut, Universität Leipzig) and external partners (ARF Lab Ohio). This serves also to benchmark our materials with respect to applications. Some of the work is performed in joint projects within GraFOx financed by the German Ministry for Research and Technology (Oxikon) and by a US MURI project. In the following we will summarize some main achievements that have been realized with MOCVD-grown homoepitaxial layers and bulk crystals grown by the Czochralski technique at IKZ. These are

(i) MOSFETs with a channel layer grown by MOVPE that showed lateral gate-drain critical field strengths of 3.8 MV/cm[1] and

(ii) RF operation with record-high transconductance at extrinsic cutoff frequency and maximum oscillating frequency of 3.3 and 12.9 GHz, respectively,[2] indicating potential for monolithic or heterogeneous integration of power switch and RF devices based on β-$Ga_2O_3$.

(iii) Wrap-gate fin-array field-effect transistors (finFETs) prepared by partial plasma etching of MOVPE β-Ga2O3 homoepitaxial layers,[3] demonstrating normally-off operation which are highly preferred for safe high-voltage operation and lower off-state power dissipation. These devices achieved an extremely high three-terminal breakdown voltage exceeding 600 V.

**MOSFET**

A two-finger MOSFET was fabricated by our colleagues at AFRL on a Sn-doped β-$Ga_2O_3$ epitaxial layer, which was grown on a Mg-doped semi-insulating bulk (100) β-$Ga_2O_3$ substrate by MOVPE at IKZ.[1] Standard DC I-V characterization was performed yielding a pinch-off voltage of −30 V giving an $I_{ON}/_{OFF}$ ratio of $10^7$. The MOSFET was found to have a $\frac{V_{BK}^2}{R_{ONSP}}$ of 11 MW/cm$^2$. An ideal device with minimal access region and contact resistance would reduce the $R_{ON} \cdot A$ product by 97%. Removing these parasitic contributions and achieving maximum μ and EC gives a $\frac{V_{BK}^2}{R_{ONSP}}$ of 24,000 MW/cm$^2$. A family of output curves was recorded with gate dielectric breakdown occurring at a total gate-to-drain voltage of −230 V. This gives a measured semiconductor field strength of 3.8 MV/cm. Sentaurus Device modelling was used to verify the field strength and calculates a lower bound for the average and maximum field strength of 3.5 MV/cm and 5.3 MV/cm respectively, across the drift region at the semiconductor/dielectric interface. This is the highest measured electric field strength in a lateral transistor and surpasses the theoretical limits of bulk SiC and GaN.

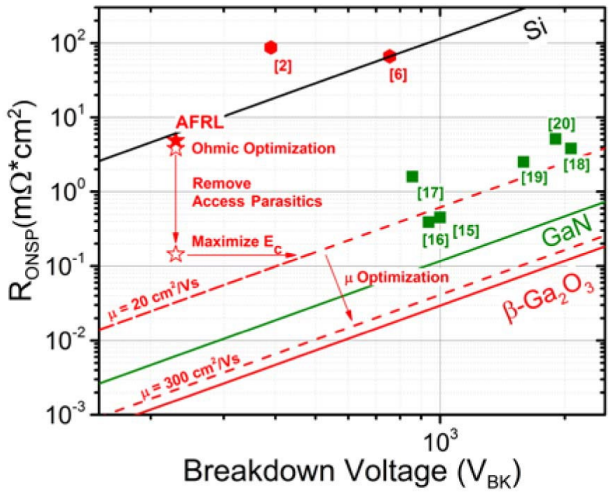


***Figure 1**. Theoretical limits for $R_{ONSP}$ vs. $V_B$ for Si, GaN, and β-$Ga_2O_3$ are plotted. The filled red star represents Ref. 1. The open stars are projections based on layout adjustments and optimization of $R_C$ $E_c$. The dashed lines represent BFOMs for a given mobility. If the mobility reaches bulk values in the low doping limit, the second dashed line would be reached. The green squares are state-of-the-art lateral GaN devices.*

**FinFET**

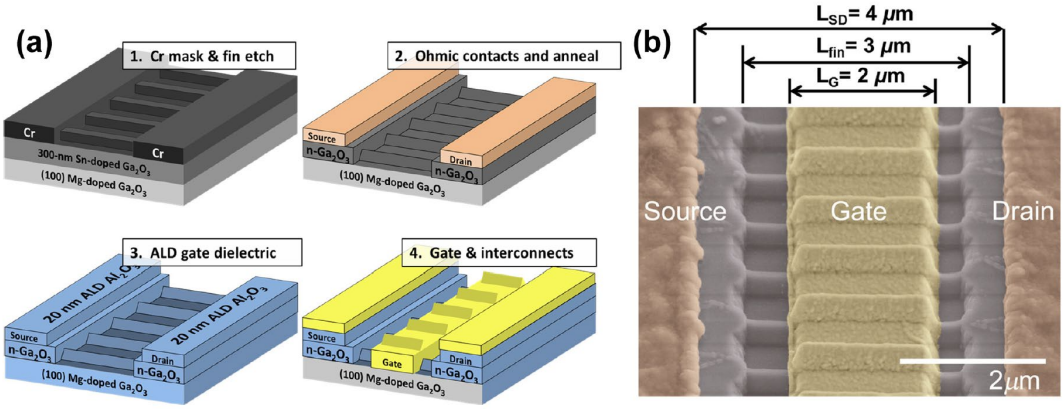


***Figure 2**. (a) Fabrication process for $Ga_2O_3$ finFETs and (b) the tilted false-colored SEM image of a $L_{SD}$ =4 μm finFET depicting the geometry of $Ga_2O_3$ fin channels and contacts.*

The first transistor devices by homoepitaxial $Ga_2O_3$ were demonstrated by NICT with a Sn-doped $Ga_2O_3$ channel grown by MBE on (010) semi-insulating β-$Ga_2O_3$ substrates.[4,5] Metal-oxide semiconductor field-effect transistors (MOSFETs) followed later with a Si-doped channel and ohmic contacts by implantation with breakdown exceeding 750-V with a fieldplate.[6,7] As shown above, Sn-doped $Ga_2O_3$ MOSFETs homoepitaxially grown by MOVPE on (100) semi-insulating β-$Ga_2O_3$ achieved a record-high 3.8 MV/cm critical field strength surpassing GaN and SiC bulk theoretical field strengths.[1] For power electronics applications, a normally-off transistor is preferred for safe high-voltage operation and to mitigate off-state power dissipation. To achieve a high current density, $Ga_2O_3$ MOSFETs require high doping concentration resulting in a negative threshold voltage ($V_{TH}$). To shift toward positive $V_{TH,}$ non-planar fin-shaped channels offer enhanced electrostatic control of the channel by depleting it from the side walls without sacrificing doping. Achieving dense, parallel arrays of fin channels is most easily achieved by top-down plasma etching. Channels formed by metal-catalyzed wet-etching and self-assembly are promising to avoid plasma etch damage.

GaN-based fin-channel field-effect transistors (finFETs) have been reported with Si-doped GaN junction less and high-electron mobility AlGaN/GaN heterostructure channels where the gate wraps around fins with enhanced electrostatics to nearly or fully deplete the channel. However, the main drawbacks for GaN are cost and the availability of native substrates for low-defect density homoepitaxial growth. In cooperation with our partners at ARFL a finFET was presented with arrays of parallel Sn-doped $Ga_2O_3$ fin channels formed by top-down plasma etching to achieve normally-off operation on a native (100) semi-insulating β-$Ga_2O_3$ substrate.[3] The results show the feasibility of wrap-gate architecture to shift the $V_{TH}$ to positive values while maintaining volume current densities for consideration in future high-voltage device design.

**RF devices**

β-$Ga_2O_3$ has recently seen significant attention as the next high-performance power electronics material. The material's ultra-wide band gap of nearly 5 eV projects an electrical breakdown strength (EC) of 8 MV/cm. While the breakdown strength is commonly applied to Baliga's figure of merit for unipolar power electronics, it also is a factor in Johnson's figure of merit (saturation velocity critical electric field product, $v_{sat} \cdot E_c$), which is used to describe the power-frequency product for RF operation. With a measured mobility as high as 100 $cm^2/V{\cdot}s$, an opportunity exists for β-$Ga_2O_3$ transistors to operate as an RF amplifier. This could have circuit level implications such as monolithic or heterogeneous device integration of high efficiency RF amplifiers, RF switches, and power switches capable of GHz switching speeds. In cooperation with the AFRL the first RF operation of a β-$Ga_2O_3$ MOSFET was demonstrated. It has been shown that β-$Ga_2O_3$ can be doped to degenerate levels with donor concentrations greater than $1 \times 10^{19}$ $cm^{-3}$.[8,9] In light of this, a highly doped capping layer was grown on a lower doped β-$Ga_2O_3$ MOSFET transistor channel permitting the combination of low ohmic contact resistance and adequate channel control with a shorter gate length through a gate recess process. These design improvements combined with improved crystalline perfection of the β-$Ga_2O_3$ layer enabled power gain measurements in both small and large signal RF operation. A cutoff frequency ($f_T$) and maximum oscillating frequency ($f_{MAX}$) of 3.3 GHz and 12.9 GHz, respectively was measured, with an output power ($P_{OUT}$) of 0.23 W/mm and a power added efficiency (PAE) of 6.3% at 800 MHz using passive source and load tuning.

**N-implantation for device isolation**

Several studies have demonstrated the successful realization of Schottky-barrier diodes and field-effect transistors based on $Ga_2O_3$ with promising results for the development of high efficiency power converters. In order to electrically isolate such electronic devices from each other, dry etching of mesa structures into the $Ga_2O_3$ is commonly carried out. On the other hand, device isolation by ion implantation was shown to be an attractive alternative on GaN-based devices as it allows to maintain the planarity of the wafer surface and thus significantly improves the yield in fine-pitch lithography. In this regard, two possible approaches of using ion implantation for inter-device isolation can be

followed. The first one relies on the creation of midgap damage-related levels which are formed by the ion bombardment causing the destruction of the crystal lattice and resulting in the trapping of free carriers in the semiconducting material. This type of compensation is stable only to the temperature at which these damage-related levels are annealed out. The second approach is based on the creation of chemically induced deep levels by implantation of a species that has an electronic level in the middle of the bandgap. Here, the implants are usually incorporated into sites in the crystal lattice, thus making annealing procedures necessary.

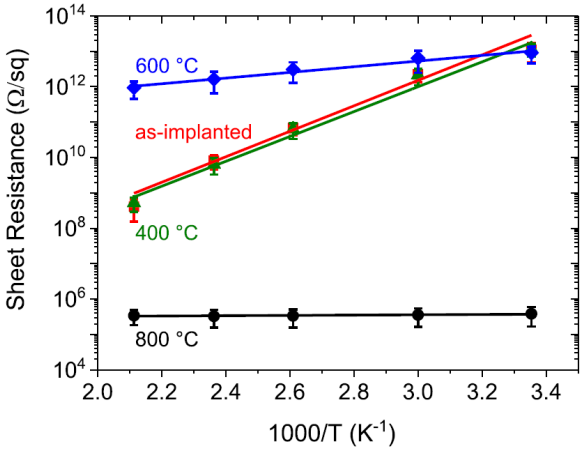


***Figure 3.*** *Arrhenius plot showing the sheet resistance $R_{SH}$ as a function of the temperature T for as-implanted and post-implantation annealed $Ga_2O_3$ samples treated at 400, 600, and 800 „C.*

This compensation effect is thermally stable under the assumption that out-diffusion or precipitation of this species does not occur. The first approach of simply disrupting the crystal lattice by the ion bombardment of nitrogen has been shown to be an effective and facile technique for the inter device isolation of several semiconducting materials such as GaAs, GaN, AlGaN, InGaN, or InP. However, the inter-device isolation by ion implantation of $Ga_2O_3$ has not yet been investigated and the effective applicability on such a material is to date still unknown. In a study that has been performed with our external partners from Ferdinand-Braun-Institut first results on the selective area isolation of $Ga_2O_3$ were presented using multiple energy $N^+$ ion implantation. This causes midgap damage-related trap levels in the semiconducting material and thus yields high sheet resistances of $10^{13}$ Ω/sq with good thermal stability up to temperatures of 600°C.[10] XRD analysis reveals the formation of structural defects after nitrogen implantation. They already start to recover at annealing temperatures of 400°C, indicating a recrystallization of the crystal lattice. This, in combination with a shift of the Fermi-level towards the conduction band with higher annealing temperatures, results in a significant drop of the sheet resistance to almost its initial value beyond 600°C (Fig. 2). The outcome of this work is an important step towards a more robust fabrication method of electronic devices based on $Ga_2O_3$ for high efficiency power electronics of the next generation.

* [1] A.J. Green, K.D. Chabak, E.R. Heller, R.C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S.E. Tetlak, A. Crespo, K. Leedy, G.H. Jessen, IEEE Electron Device Lett. **37**, 902 (2016). DOI: 10.1109/LED.2016.2568139

* [2] A.J. Green, K.D. Chabak, M. Baldini, N. Moser, R. Gilbert, R.C. Fitch, G. Wagner, Z. Galazka, J. Mccandless, A. Crespo, K. Leedy, G.H. Jessen, IEEE Electron Device Lett. **38,** 790 (2017). DOI: 10.1109/LED.2017.2694805

* [3] Kelson D. Chabak, N. Moser, A. J. Green, D. E. Walker, S. E. Tetlak, E. Heller, A. Crespo, R. Fitch, J. P. McCandless , K. Leedy, M. Baldini, G. Wagner, Z. Galazka, X. Li, and G. Jessen, Appl. Phys. Lett. **109**, 213501 (2016). DOI: 10.1063/1.4967931

[4] M. Higashiwaki, K. Sasaki, T. Kamimura, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, Appl. Phys. Lett. **103**, 123511 (2013). DOI: 10.1063/1.4821858

[5] H. Murakami, K. Nomura, K. Goto, K. Sasaki, K. Kawara, Q. T. Thieu, R. Togashi, Y. Kumagai, M. Higashiwaki, and A. Kuramata, Appl. Phys. Express **8**, 015503 (2015). DOI: 10.7567/APEX.8.015503

[6] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, Appl. Phys. Express **6**, 086502 (2013). DOI: 10.7567/APEX.6.086502

[7] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, IEEE Electron Device Lett. **37**, 212 (2016). DOI: 10.1109/LED.2015.2512279

[8] K. Sasaki, A. Kuramata, T. Masui, E. G. Villora, K. Shimamura, and S. Yamakoshi, Appl. Phys. Exp. **5**, 035502 (2012). DOI: 10.1143/APEX.5.035502

* [9] M. Baldini, M. Albrecht, A. Fiedler, K. Irmscher, R. Schewski, and G. Wagner, ECS J. Solid State Sci. Technol. **6**, Q3040 (2017). DOI: 10.1149/2.0081702jss

* [10] K. Tetzner, A. Thies, E. Bahat Treidel, F. Brunner, G. Wagner, and J.Würfl, Appl. Phys. Lett. **113**, 172104 (2018). DOI: 10.1063/1.5046139


**GraFox publications are highlighted by an "*".**